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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,882	09/30/2003	Randy B. Osborne	42P16963	8106

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EXAMINER	
SCHLIE, PAUL W	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,882	OSBORNE, RANDY B.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) *5-6, 18, 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 7-17 and 19-21* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/30/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined as amended, where claims 5-6, 18 and 22 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 3/3/06 with respect to the objection to the drawings based on claim 6 (being now canceled), and objections to claims 2, 5 and 20 (being now either amended or canceled) has been fully considered and are persuasive; thereby the objections have been correspondingly withdrawn.

3. Applicant's arguments with respect to claims 3-6, 13-14, 17-18 and 21-22 rejection under 35 U.S.C 112 has been fully considered and are partially persuasive in view of claims 5-6, 18 and 22 being withdrawn and claims 3-4, 13-14, 17 and 21 being amended; as detailed in the correspondingly amended 35 U.S.C. 112 rejection below.

4. Applicant's remaining arguments have been fully considered but they are not persuasive.

As per claim 1 rejected under 35 U.S.C 102, in consideration of the arguments, the rejection has been clarified by identifying locations more clearly implicitly covering the claims within the reference cited, although the claims are considered clearly known by those of ordinary skill in the art as all conventional DRAM implementations inherently close a presently open row in response to a request to open a different row within the same memory bank (as it is correspondingly physically impossible for more than a single row within a single bank to be open simultaneously within a conventional single port DRAM bank implementation), and further as it is correspondingly well understood

that no rows (or a unspecified row) are/is correspondingly activated upon a bank being activated (i.e. pre-charged/powered), all claims are correspondingly inherent within all conventional DRAM implementations; thereby the rejection is sustained. (Where as an aside, although not explicitly claimed, the reference explicitly teaches the means by which row activate commands need not be preceded by an explicit bank pre-charge as detailed within column 23 lines 13-30 and corresponding schematic diagram figures, which correspondingly implicitly teaches that an existing open row within any single bank is inherently closed in response to the request to open a different row within any single bank as there is only one row address register and corresponding decode logic associated with each memory bank).

As per claim 2 rejected under 35 U.S.C 103, as no specific elements of the claim were contested and presented for reconsideration, the rejection is sustained.

Claim Objections

5. Claim 7 is objected to, as although a controlling device may contain a "memory device" as amended, it has introduced an inconsistency; as "memory device" within the context of the application and claims otherwise consistently refer to a memory device which is distinct and the object of the controllers actions, not what may be arguably more appropriately considered storage registers within the controller itself as the previous structure of the claim more clearly implied. The claim will be interpreted as previously interpreted. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

More specifically, no facility or mechanism has been disclosed or detailed within the drawings to enable a memory device as claimed to provide an indication that is readable by another device of its ability to support a particular mode of operation; the claim is not considered sufficiently enabled to enable one of ordinary skill in the art to make or use the claimed invention, unless considered otherwise obvious.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States..

9. Claim 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe (5,463,590).

As per claims 1 and 3, Watanabe teaches a memory device comprising: at least one bank comprised of memory cells organized by rows and columns; control logic where in response to a row activate command will close a previously open row, and open the row requested, were upon receipt of an explicit bank pre-charge command

effectively closes any previously oven row within that bank (see column 23 lines 13-30, table 6, and figure 1 elements 32/33 and 57, and figure 1, which correspondingly implicitly teaches that an existing open row within any single bank is inherently closed in response to the request to open a different row within any single bank or upon an explicit receipt of a bank pre-charge command, as there is only one row/bank address register and corresponding decode logic associated with each memory bank, as considered to be commonly understood by those of ordinary skill in the art at the time of the claimed invention).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590) in further in view of Osborne (US App.10/676,882) and Bondurant et al. (6,330,636).

As per claim 2, Watanabe teaches claim 1 (as above), but does not teach that data may be transferred across the data bus synchronized to twice the clock rate of the device. However Osborne acknowledges DDR "Double Data Rate" DRAM as prior art within the Background of the application, see page 3 lines 16-18, as is also taught by Bondurant et al. (also teaching that DDR DRAM memory devices tend to support the mode of operation as in claim 1). Therefore it would be obvious to one of ordinary skill

in the art to combine DDR transfer capabilities as taught by Osborne with the memory as taught by Watanabe, to reduce the latency of multi-cycle memory data transactions.

12. Claims 7-17, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590), Osborne (US App.10/676,882) and Bondurant et al. (6,330,636) in further view of "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" second edition, as published 10/2002 in English, and 8/2002 in Japanese, and Schaefer (5,636,173).

As per claims 7-17 and 19-21, Watanabe, Osborne and Bondurant et al. teach a controller interconnected with a memory device comprising: at least one bank comprised of memory cells organized by rows and columns; control logic where in response to a row activate command will close a previously open row, and open the row requested, similarly to claims 1-2; however does not teach a computer system comprised of such a memory device, a processor, and memory controller capable of tracking as many as two different storage locations contained within a memory device such that upon a request potentially necessitating the activation of a row, it may be determined if the presence of an open row will corresponding necessitate the closing/pre-charging a currently open row such that all correspondingly required delay timing requirements of the memory device, nor that an auto-pre-charge may be implicitly previously conducted upon a request for a transaction from a row different from the row presently being requested to active (where such requirements may be determined upon access to a corresponding memory parameter data memory associated with said memory as is commonly known to those of ordinary skill in the art at the time of the

claimed invention). "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teaches a computer system comprising a processor and memory which can determine if a pre-charge command/delay is required to be accounted for in response to a request for a memory transaction from a row which may differ from a previously open row, see pages 22, 26, and 59; and Schaefer teaches a memory bank may be implicitly auto-pre-charged in response to a row transaction in preparation for a subsequent row activation (where such information is considered inherently stored within such a controller within accessible registers), see figure 2 and page 1 abstract lines 10-13. It would have been obvious to one of ordinary skill in the art to combine tat taught as referenced above relevant to the claims for the benefit of potentially improving memory transaction performance and efficiency of such a system.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765, or whose email address is [paul.schlie@uspto.gov]. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
3\17\06